REMARKS

Claim Rejections Under 35 U.S.C. § 102

Claims 4, 5, 9-12, 14, 15-16, 18, 19, 20, 23-25, 26-29, 32, 33-38, 42-46 and 48 were rejected under 35 U.S.C. § 102(e) as being anticipated by Itoh et al. (U. S. Patent No. 5,966,720). Applicant notes that the issue date of Itoh et al. (October 12, 1999) is more than one year before the filing date of the Specification (August 24, 2001). The Applicant therefore respectfully submits that the Examiner's rejection is more properly placed under 35 U.S.C. § 102(b). Applicant respectfully traverses this rejection and feels that claims 4, 5, 9-12, 14, 15-16, 18, 19, 20, 23-25, 26-29, 32, 33-38, 42-46 and 48 are allowable for the following reasons.

Applicant respectfully maintains that Itoh et al. teaches a memory which has sector management data structure stored in each sector of an erase block that describes the sector's status and logical address within the erase block. Applicant notes that Itoh et al.'s sector management structure does not correspond to Applicant's block management data structure as Itoh et al.'s structure cannot manage status or availability of an entire block, but only a subsection. *See, e.g.*, Itoh et al., Figure 1, Element B(Block), Figure 3, column 4, lines 8-28, column 1, lines 30-53, and column 2, line 54 to column 3, line 13. The Specification of the Present Application defines an erase block as a section of a flash memory having multiple logical sectors that can be randomly accessed and programmed, but the erase block must be erased as a single unit. Erase block management is defined as providing an abstraction layer to allow for the flash memory to appear as a freely rewrite-able device, logically remap the addresses of the erase blocks, and allow block erase operations to occur. The Specification of the Present Application also defines erase block data management data as the summary erase block management data, such as available (erased) blocks, invalid blocks available to be erased, erase block logical to physical address mapping, valid (full) blocks, and partially full blocks. *See, e.g.*, Specification, Figures 1 and 2, Paragraphs 4-6, 9, 11, 40, 42, 51-52 and 54-55. Applicant therefore respectfully submits that Itoh et al. does not teach or disclose storing an erase block management data structure in each erase block of a plurality of erase blocks of a non-volatile memory array.

Applicant's claim 4 is directed to a Flash memory device comprising a memory array containing a plurality of floating gate memory cells arranged in a plurality of erase blocks, wherein each of the plurality of erase blocks is further arranged into a plurality of sectors, each

sector of the plurality of sectors having a user data section and a control data section, and an erase block management data structure arranged in the control data sections of a subset of sectors of each erase block of the plurality of erase blocks. As detailed above, Applicant submits that Itoh et al. fails to teach or disclose such a Flash memory device having an erase block management data structure. As such, Itoh et al. fails to teach or disclose all elements of independent claim 4.

Applicant's claim 9 is directed to a Flash memory device comprising a memory array containing a plurality of floating gate memory cells divided into a plurality of erase blocks, wherein each of the plurality of erase blocks is further divided into a plurality of sectors, each sector of the plurality of sectors having a user data section and a control data section, and an erase block management data structure arranged in the control data sections of a first set of sectors of each erase block of the plurality of erase blocks. As detailed above, Applicant submits that Itoh et al. fails to teach or disclose such a Flash memory device having an erase block management data structure. As such, Itoh et al. fails to teach or disclose all elements of independent claim 9.

Applicant's claim 15 is directed to a Flash memory device comprising a memory array containing a plurality of floating gate memory cells arranged in a plurality of erase blocks, wherein each of the plurality of erase blocks is further divided into a plurality of sectors, each sector of the plurality of sectors having a user data section and a control data section, and an erase block management data structure arranged in the control data sections of a subset of sectors of each erase block of the plurality of erase blocks, wherein each erase block of the plurality of erase blocks has an erase block state that is recorded in the erase block management data structure of the erase block. As detailed above, Applicant submits that Itoh et al. fails to teach or disclose such a Flash memory device having an erase block management data structure. As such, Itoh et al. fails to teach or disclose all elements of independent claim 15.

Applicant's claim 20 is directed to a Flash memory device comprising a memory array containing a plurality of floating gate memory cells arranged in a plurality of erase blocks, wherein each of the plurality of erase blocks is further divided into a plurality of sectors, each sector of the plurality of sectors having a user data section and a control data section, a control circuit, and an erase block management data structure arranged in the control data sections of a first set of sectors of each erase block of the plurality of erase blocks. As detailed above, Applicant submits that Itoh et al. fails to teach or disclose such a Flash memory device having an

erase block management data structure. As such, Itoh et al. fails to teach or disclose all elements of independent claim 20.

Applicant's claim 26 is directed to a system comprising a host coupled to a Flash memory device. The Flash memory device comprising a memory array containing a plurality of floating gate memory cells arranged in a plurality of erase blocks, wherein each of the plurality of erase blocks is further divided into a plurality of sectors, each sector of the plurality of sectors having a user data section and a control data section, and an erase block management data structure arranged in the control data sections of a subset of sectors of each erase block of the plurality of erase blocks. As detailed above, Applicant submits that Itoh et al. fails to teach or disclose such a system and Flash memory device having an erase block management data structure. As such, Itoh et al. fails to teach or disclose all elements of independent claim 26.

Applicant's claim 32 is directed to a method of making a Flash memory device comprising forming a memory array containing a plurality of floating gate memory cells arranged in a plurality of erase blocks, wherein each of the plurality of erase blocks is further divided into a plurality of sectors, each sector of the plurality of sectors having a user data section and a control data section, and forming an erase block management data structure in the control data sections of a subset of sectors of each erase block of the plurality of erase blocks. As detailed above, Applicant submits that Itoh et al. fails to teach or disclose such a method. As such, Itoh et al. fails to teach or disclose all elements of independent claim 32.

Applicant's claim 33 is directed to a method of operating a Flash memory device comprising storing an erase block management data structure in each erase block of a plurality of erase blocks of a Flash memory array, wherein each erase block contains a plurality of sectors and the erase block management data structure of each erase block is stored in a plurality of control data sections of a subset of the plurality of sectors. As detailed above, Applicant submits that Itoh et al. fails to teach or disclose such a method. As such, Itoh et al. fails to teach or disclose all elements of independent claim 33.

Applicant's claim 42 is directed to a method of operating a Flash memory device comprising placing an erase block management data structure in a control data section of a subset of sectors of a plurality of sectors of each erase block of a plurality of erase blocks of a Flash memory array, and recording an erase block state in the erase block management data structure in the control data section of the subset of sectors of each erase block of the plurality of

erase blocks. As detailed above, Applicant submits that Itoh et al. fails to teach or disclose such a method. As such, Itoh et al. fails to teach or disclose all elements of independent claim 42.

Applicant respectfully contends that claims 4, 9, 15, 20, 26, 32, 33 and 42 have been shown to be patentably distinct from the cited reference. As claims 5, 10-12, 14, 16, 18-19, 23-25, 27-29, 34-38, 43-46 and 48 depend from and further define claims 4, 9, 15, 20, 26, 32, 33 and 42, respectively, they are also considered to be in condition for allowance. Accordingly, Applicant respectfully requests withdrawal of the rejection under 35 U.S.C. § 102(b) and allowance of claims 4, 5, 9-12, 14, 15-16, 18, 19, 20, 23-25, 26-29, 32, 33-38, 42-46 and 48.

Claims 4, 9, 15, 20, 26, 32, 33 and 42 were rejected under 35 U.S.C. § 102(a) as being anticipated by Applicant's Admitted Prior Art (AAPA). Applicant respectfully traverses this rejection and feels that claims 4, 9, 15, 20, 26, 32, 33 and 42 are allowable for the following reasons.

Applicant respectfully maintains that the AAPA of Figure 1 teaches a Flash memory which stores erase block management data in non-volatile erase block management registers and tables 128 that are separate from the erase blocks 116 and their sectors 120. The Applicant respectfully maintains that the element 122, relied upon by the Examiner as an erase block management data structure, refers to a sector control data space 122 for use with management of the associated sector 118. The Specification states in reference to Figure 1, "[t]he RAM control registers and tables 114 are loaded at power up from the non-volatile erase block management registers and tables 128 by the control state machine 110. The Flash memory array 112 contains a sequence of erase blocks 116. Each erase block 116 contains a series of sectors 118 that include a user data space 120 and a control data space 122. The control data space 122 contains overhead information for operation of the sector, such as an error correction code (not shown)." *See, e.g.*, Specification, Figure 1 and Paragraph 11. Applicant therefore respectfully submits that the AAPA does not teach or disclose a non-volatile memory device which stores an erase block management data structure in each erase block of a plurality of erase blocks of a non-volatile memory array.

Applicant's claim 4 is directed to a Flash memory device comprising a memory array containing a plurality of floating gate memory cells arranged in a plurality of erase blocks, wherein each of the plurality of erase blocks is further arranged into a plurality of sectors, each

sector of the plurality of sectors having a user data section and a control data section, and an erase block management data structure arranged in the control data sections of a subset of sectors of each erase block of the plurality of erase blocks. As detailed above, Applicant submits that the AAPA fails to teach or disclose such a Flash memory device having an erase block management data structure. As such, the AAPA fails to teach or disclose all elements of independent claim 4.

Applicant's claim 9 is directed to a Flash memory device comprising a memory array containing a plurality of floating gate memory cells divided into a plurality of erase blocks, wherein each of the plurality of erase blocks is further divided into a plurality of sectors, each sector of the plurality of sectors having a user data section and a control data section, and an erase block management data structure arranged in the control data sections of a first set of sectors of each erase block of the plurality of erase blocks. As detailed above, Applicant submits that the AAPA fails to teach or disclose such a Flash memory device having an erase block management data structure. As such, the AAPA fails to teach or disclose all elements of independent claim 9.

Applicant's claim 15 is directed to a Flash memory device comprising a memory array containing a plurality of floating gate memory cells arranged in a plurality of erase blocks, wherein each of the plurality of erase blocks is further divided into a plurality of sectors, each sector of the plurality of sectors having a user data section and a control data section, and an erase block management data structure arranged in the control data sections of a subset of sectors of each erase block of the plurality of erase blocks, wherein each erase block of the plurality of erase blocks has an erase block state that is recorded in the erase block management data structure of the erase block. As detailed above, Applicant submits that the AAPA fails to teach or disclose such a Flash memory device having an erase block management data structure. As such, the AAPA fails to teach or disclose all elements of independent claim 15.

Applicant's claim 20 is directed to a Flash memory device comprising a memory array containing a plurality of floating gate memory cells arranged in a plurality of erase blocks, wherein each of the plurality of erase blocks is further divided into a plurality of sectors, each sector of the plurality of sectors having a user data section and a control data section, a control circuit, and an erase block management data structure arranged in the control data sections of a first set of sectors of each erase block of the plurality of erase blocks. As detailed above, Applicant submits that the AAPA fails to teach or disclose such a Flash memory device having

an erase block management data structure. As such, the AAPA fails to teach or disclose all elements of independent claim 20.

Applicant's claim 26 is directed to a system comprising a host coupled to a Flash memory device. The Flash memory device comprising a memory array containing a plurality of floating gate memory cells arranged in a plurality of erase blocks, wherein each of the plurality of erase blocks is further divided into a plurality of sectors, each sector of the plurality of sectors having a user data section and a control data section, and an erase block management data structure arranged in the control data sections of a subset of sectors of each erase block of the plurality of erase blocks. As detailed above, Applicant submits that the AAPA fails to teach or disclose such a system and Flash memory device having an erase block management data structure. As such, the AAPA fails to teach or disclose all elements of independent claim 26.

Applicant's claim 32 is directed to a method of making a Flash memory device comprising forming a memory array containing a plurality of floating gate memory cells arranged in a plurality of erase blocks, wherein each of the plurality of erase blocks is further divided into a plurality of sectors, each sector of the plurality of sectors having a user data section and a control data section, and forming an erase block management data structure in the control data sections of a subset of sectors of each erase block of the plurality of erase blocks. As detailed above, Applicant submits that the AAPA fails to teach or disclose such a method. As such, the AAPA fails to teach or disclose all elements of independent claim 32.

Applicant's claim 33 is directed to a method of operating a Flash memory device comprising storing an erase block management data structure in each erase block of a plurality of erase blocks of a Flash memory array, wherein each erase block contains a plurality of sectors and the erase block management data structure of each erase block is stored in a plurality of control data sections of a subset of the plurality of sectors. As detailed above, Applicant submits that the AAPA fails to teach or disclose such a method. As such, the AAPA fails to teach or disclose all elements of independent claim 33.

Applicant's claim 42 is directed to a method of operating a Flash memory device comprising placing an erase block management data structure in a control data section of a subset of sectors of a plurality of sectors of each erase block of a plurality of erase blocks of a Flash memory array, and recording an erase block state in the erase block management data structure in the control data section of the subset of sectors of each erase block of the plurality of

erase blocks. As detailed above, Applicant submits that the AAPA fails to teach or disclose such a method. As such, the AAPA fails to teach or disclose all elements of independent claim 42.

Applicant respectfully contends that claims 4, 9, 15, 20, 26, 32, 33 and 42 have been shown to be patentably distinct from the cited reference. Accordingly, Applicant respectfully requests withdrawal of the rejection under 35 U.S.C. § 102(a) and allowance of claims 4, 9, 15, 20, 26, 32, 33 and 42.

Claim Rejections Under 35 U.S.C. § 103

Claims 6, 8, 39 and 41 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Itoh, et al., in view of Reasoner, et al. (U. S. Patent No. 5,608,684). Applicant respectfully traverses this rejection and feels that claims 6, 8, 39 and 41 are allowable for the following reasons.

Applicant respectfully notes that, as stated above in regards to the rejection of independent claim 4, from which claims 6 and 8 depend, Itoh et al. fails to teach a Flash memory that has an erase block management data structure that resides in the control data sections of a subset of sectors of each erase block. As such, Itoh et al. fails to teach or disclose independent claim 4 and therefore does not teach or suggest all elements of claims 6 and 8. In addition, Reasoner et al. also does not teach an erase block management data structure that resides in the control data sections of a subset of sectors of each erase block. Therefore combining the elements of Itoh et al. with Reasoner et al. does not teach or suggest all elements of claim 4. The Applicant therefore maintains that claim 4 is thus allowable over Itoh et al. and Reasoner et al., either alone or in combination. As claims 6 and 8 depend from and further define claim 4, claims 6 and 8 are also deemed allowable.

In regards to independent claim 39, the Applicant respectfully submits that, as stated above, Itoh et al. fails to teach a Flash memory that has an erase block management data structure that resides in the control data sections of a subset of sectors of each erase block. As such, Itoh et al. fails to teach or suggest all elements of claim 39. In addition, Reasoner et al. also does not teach an erase block management data structure that resides in the control data sections of a subset of sectors of each erase block. Therefore combining the elements of Itoh et al. with Reasoner et al. does not teach or suggest all elements of claim 39. The Applicant therefore maintains that claim 39 is thus allowable over Itoh et al. and Reasoner et al., either

alone or in combination. As claim 41 depends from and further defines claim 39, claim 41 is also deemed allowable.

Applicant respectfully contends that claims 6, 8, 39 and 41 as pending have been shown to be patentably distinct from the cited references, either alone or in combination. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection under 35 U.S.C. § 103(a) and allowance of claims 6, 8, 39 and 41.

Claims 7 and 40 were rejected under 35 U. S. C. § 103(a) as being unpatentable over Itoh et al., in view of Reasoner et al., and further in view of Duke (U. S. Patent 3,576,982). Applicant respectfully traverses this rejection and feels that claims 7 and 40 are allowable for the following reasons.

Applicant respectfully notes that, as stated above in regards to the rejection of independent claims 4 and 39 which claims 7 and 40 depend from, Itoh et al. fails to teach a Flash memory that has an erase block management data structure that resides in the control data sections of a subset of sectors of each erase block. As such, Itoh et al. fails to teach or suggest independent claims 4 and 39 and therefore does not teach or suggest all elements of claims 7 and 40. In addition, Reasoner et al. and Duke do not teach an erase block management data structure that resides in the control data sections of a subset of sectors of each erase block. Therefore combining the elements of Itoh et al. with Reasoner et al. and Duke does not teach or suggest all elements of claims 4 and 39. The Applicant therefore maintains that claims 4 and 39 are thus allowable over Itoh et al., Reasoner et al. and Duke, either alone or in combination. As claims 7 and 40 depend from and further define claims 4 and 39, claims 7 and 40 are also deemed allowable.

Applicant respectfully contends that claims 7 and 40 as pending have been shown to be patentably distinct from the cited references, either alone or in combination. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection under 35 U.S.C. § 103(a) and allowance of claims 7 and 40.

Claims 22, 21 and 49 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Itoh et al. in view of AAPA. Applicant respectfully traverses this rejection and feels that claims 22, 21 and 49 are allowable for the following reasons.

Applicant respectfully notes that, as stated above in regards to the rejection of independent claims 20 and 42 which claims 22, 21 and 49 depend from, Itoh et al. fails to teach a Flash memory that has an erase block management data structure that resides in the control data sections of a subset of sectors of each erase block. As such, Itoh et al. fails to teach or suggest independent claims 20 and 42 and therefore does not teach or suggest all elements of claims 22, 21 and 49. In addition, as also stated above, the AAPA does not teach an erase block management data structure that resides in the control data sections of a subset of sectors of each erase block. Therefore combining the elements of Itoh et al. with the AAPA does not teach or suggest all elements of claims 20 and 42. The Applicant therefore maintains that claims 20 and 42 are thus allowable over Itoh et al., Reasoner et al. and Duke, either alone or in combination. As claims 22, 21 and 49 depend from and further define claims 20 and 42, claims 22, 21 and 49 are also deemed allowable.

Applicant respectfully contends that claims 22, 21 and 49 as pending have been shown to be patentably distinct from the cited references, either alone or in combination. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection under 35 U.S.C. § 103(a) and allowance of claims 22, 21 and 49.

Claims 1 and 3 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Applicant's Admitted Prior Art (AAPA) in view of Itoh et al. Applicant respectfully traverses this rejection and feels that claims 1 and 3 are allowable for the following reasons.

The Applicant respectfully submits that, as stated above, Itoh et al. fails to teach a Flash memory that has an erase block management data structure that resides in the control data sections of a subset of sectors of each erase block. As such, Itoh et al. fails to teach or suggest all elements of independent claim 1. In addition, as also stated above, the AAPA does not teach an erase block management data structure that resides in the control data sections of a subset of sectors of each erase block. Therefore combining the elements of Itoh et al. with the AAPA does not teach or suggest all elements of claim 1. The Applicant therefore maintains that claim 1 is thus allowable over Itoh et al. and the AAPA, either alone or in combination. As claim 3 depends from and further defines claim 1, claim 3 is also deemed allowable.

Applicant respectfully contends that claims 1 and 3 as pending have been shown to be

patentably distinct from the cited references, either alone or in combination. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection under 35 U.S.C. § 103(a) and allowance of claims 1 and 3.

Claim 2 was rejected under 35 U.S.C. § 103(a) as being unpatentable over AAPA in view of Itoh et al., and further in view of Duke. Applicant respectfully traverses this rejection and feels that claim 2 is allowable for the following reasons.

The Applicant respectfully submits that, as stated above in regards to claim 1 which claim 2 depends from, Itoh et al. fails to teach a Flash memory that has an erase block management data structure that resides in the control data sections of a subset of sectors of each erase block. As such, Itoh et al. fails to teach or suggest all elements of independent claim 1. In addition, as also stated above, the AAPA and Duke do not teach an erase block management data structure that resides in the control data sections of a subset of sectors of each erase block. Therefore combining the elements of Itoh et al. with the AAPA and Duke do not teach or suggest all elements of claim 1. The Applicant therefore maintains that claim 1 is thus allowable over Itoh et al., the AAPA and Duke, either alone or in combination. As claim 2 depends from and further defines claim 1, claim 2 is deemed allowable.

Applicant respectfully contends that claim 2 as pending have been shown to be patentably distinct from the cited references, either alone or in combination. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection under 35 U.S.C. § 103(a) and allowance of claim 2.

Claims 17, 30-31, 47 and 50-51 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Itoh et al. in view of AAPA. Applicant respectfully traverses this rejection and feels that claims 17, 30-31, 47 and 50-51 are allowable for the following reasons.

The Applicant respectfully submits that, as stated above, Itoh et al. fails to teach a Flash memory that has an erase block management data structure that resides in the control data sections of a subset of sectors of each erase block. As such, Itoh et al. fails to teach or suggest all elements of independent claims 15, 26, 42 and 50. In addition, as also stated above, the AAPA does not teach an erase block management data structure that resides in the control data sections

of a subset of sectors of each erase block. Therefore combining the elements of Itoh et al. with the AAPA does not teach or suggest all elements of claims 15, 26, 42 and 50. The Applicant therefore maintains that claims 15, 26, 42 and 50 are thus allowable over Itoh et al. and the AAPA, either alone or in combination. As claims 17, 30-31, 47 and 51 depend from and further defines claims 15, 26, 42 and 50, claims 17, 30-31, 47 and 51 are also deemed allowable.

Applicant respectfully contends that claims 17, 30-31, 47 and 50-51 as pending have been shown to be patentably distinct from the cited references, either alone or in combination. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection under 35 U.S.C. § 103(a) and allowance of claims 17, 30-31, 47 and 50-51.

CONCLUSION

In view of the above remarks, Applicant respectfully submits that the claims are in condition for allowance and requests reconsideration of the application and allowance of the claims. No new matter has been added and no additional fee is required by this amendment and response.

The Examiner is invited to contact Applicant's representative at (612) 312-2207 if there are any questions regarding this response or if prosecution of this application may be assisted thereby.

Respectfully submitted,

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Andrew C. Walseth
Reg. No. 43,234

Attorneys for Applicant
Leffert Jay & Polglaze
P.O. Box 581009
Minneapolis, MN 55458-1009
T 612 312-2200
F 612 312-2250